IN THE CLAIMS

1. (*Previously Presented*) A process for forming a contact for a semiconductor device comprising:

forming a first compound semiconductor layer, wherein: the first compound semiconductor material layer includes a first compound semiconductor material and has a first conductivity type;

forming a second compound semiconductor layer, wherein the second compound semiconductor layer includes a second compound semiconductor material and has a second conductivity type; and the second conductivity type is opposite the first conductivity type;

patterning the second semiconductor layer to define an opening therein with a wall, said opening exposing a portion of the first active layer; and

forming a third compound semiconductor material upon at least a portion of the exposed first active layer and at least partially within the opening, wherein: the third compound semiconductor material has an upper surface that is substantially co-planar with an upper surface of the second compound semiconductor layer, has the first conductivity type and a dopant concentration that is higher than a dopant concentration of the first compound semiconductor layer; and the third compound semiconductor material is electrically connected to the first compound semiconductor layer and is insulated from the second compound semiconductor layer.

2. (*Original*) The process of claim 1, wherein the third compound semiconductor material is formed by sputtering.

3. (*Original*) The process of claim 1, wherein each of the first, second, and third compound semiconductor materials include at least two Group IVA elements.

4. (*Original*) The process of claim 1, wherein each of the first, second, and third compound semiconductor materials include silicon carbide.

5. (*Original*) The process of claim 1, further comprising forming a metal layer above and electrically connected to the third compound semiconductor material.

6. (*Original*) The process of claim 5, wherein an electrical connection between the third compound semiconductor material and the metal layer is ohmic.

7. (*Original*) The process of claim 5, wherein the metal layer comprises aluminum.

8. (*Previously Presented*) The process of claim 1 further comprising forming a fourth compound semiconductor layer before forming the first compound semiconductor layer, wherein the fourth compound semiconductor layer includes a fourth compound semiconductor material and has the second conductivity type.

9. (*Previously Presented*) A semiconductor device comprising:

a first active layer including a first compound semiconductor material and having a first conductivity type;

a second active layer including a second compound semiconductor material and having a second conductivity type opposite the first conductivity type, wherein the second active layer contacts the first active layer;

a third active layer including a third compound semiconductor material and having the first conductivity type, wherein the third active layer contacts the second active layer, a combination of the first, second, and third active layer are at least part of a transistor;

an opening defined by said second and third active layers, said opening extending through the third active layer, said opening contacting and terminating within the second active layer;

a fourth compound semiconductor material at least partially within the opening, wherein the fourth compound semiconductor material has the second conductivity type and a dopant concentration higher than the dopant concentration of the second active layer and is electrically connected to the second active layer, the fourth compound semiconductor material having an upper surface that is substantially coplanar with an upper surface of the third compound semiconductor layer; and

an insulating layer at least partially within the opening, wherein the insulating layer lies between the third active layer and the fourth compound semiconductor material.

10. (*Original*) The device of claim 9, where each of the first, second, third, and fourth compound semiconductor material include at least two Group IVA elements.

11. (*Original*) The device of claim 9, where the first, second, third, and fourth compound semiconductor material comprise silicon carbide.

12. (*Original*) The device of claim 9, further comprising electrical contacts to the third active layer and the fourth compound semiconductor material.

13. (*Original*) The device of claim 12, wherein the electrical contacts are ohmic.

14. (*Previously Presented*) The device of claim 13, wherein the device further comprises a second insulating layer on the surface of the third active layer and surfaces of the second insulating layer and the metal contacts furthest from the substrate lie in substantially a same plane.

15. (*Original*) The device of claim 9, wherein the second active layer has a thickness in a range of approximately 0.1 - 2 microns thick.

16. (*Previously Presented*) A semiconductor device comprising:

a first active layer including a first compound semiconductor material and having a first conductivity type;

a second active layer including a second compound semiconductor material and having a second conductivity type opposite the first conductivity type, wherein the second active layer contacts the first active layer;

a third active layer including a third compound semiconductor material and having the first conductivity type, wherein the third active layer contacts the second active layer, a combination of the first, second, and third active layer are at least part of a transistor;

an opening defined by the second and third active layers, the opening extending through the third active layer, the opening terminating within and exposing a portion of the second active layer, sidewalls of the opening formed by the third active layer, a bottom of the opening formed by the exposed portion of the second active layer;

an insulating layer at least partially within the opening and covering the sidewalls thereof; and

a fourth compound semiconductor material disposed within the opening upon the exposed portion of the second active layer and upon the insulating layer covering the sidewalls thereof, the fourth compound semiconductor material having the second conductivity type and a dopant concentration higher than the dopant concentration of the second active layer and being electrically connected to the second active layer, the fourth compound semiconductor material substantially filling the opening and having an upper surface that is substantially coplanar with an upper surface of the third compound semiconductor layer.